REMARKS

Claim 6 was rejected under 35 U.S.C 112, second paragraph as having no antecedent basis for the limitation of "the differential amplifier". Claim 6 is amended herein to correct this deficiency.

Claims 1-9, 12, and 14 were rejected under 35 U.S.C. 102(e) as allegedly anticipated by *Tsuchi* (USP 6614295). Claims 10 and 11 were rejected under 35 U.S.C. 103(a) as allegedly unpatentable over *Tsuchi* in view of *Forbes* (USP 6362691). Claim 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Tsuchi* in view of *Khalid* (US 2004/0150464). For at least the reasons set forth herein, Applicant respectfully requests reconsideration of these rejections.

Discussion of Rejections Under 35 U.S.C. 102(e)

As to the rejection under 35 U.S.C. 102(e), please note that "the broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach." *In re Cortright*, 165 F.3d 1353, 1359, 49 USPQ2d 1464, 1468 (Fed. Cir. 1999) Below is the original independent claim 1 of this application.

> 1. A voltage reference generator for generating an output voltage at an output node, comprising:
>
> a level shifter for shifting **a first reference voltage** into the output voltage at the output node according to a shift between the first reference voltage and the output voltage; and
>
> a feedback circuit for monitoring the output voltage and **a second reference voltage** to control the shift and to normalized the output and second reference voltages.

(*Emphasis added*).

The Office Action cites Fig. 10 of *Tsuchi* as an allegedly anticipatory reference to reject claim 1 under 35 U.S.C. 102(e). However, *Tsuchi* teaches no first and second reference voltages,

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as required by claim 1. Since there is at least one limitation of claim 1 absent in the cited prior art, the rejection should be withdrawn.

The Office Action interprets the gate voltage of MOS 422 and the voltage of Vin in Fig. 10 of *Tsuchi* as the first and second reference voltages in claim 1 of the present application. Referring to "FIELD OF THE INVENTION" of *Tsuchi*, however, *Tsuchi* teaches a "driving circuit capable of driving a data line of a capacitive load at a high speed ... in an active matrix display device". It is obvious for persons skilled in that art that, in *Tsuchi*, the voltage of Vin always and frequently varies because data sent to a data line of an active matrix display device always changes. The gate voltage of MOS 422 also varies as long as voltage of Vin varies according to circuit operation in Fig. 10 of *Tsuchi*. For those skilled in the art, reference voltages, in contrast, are used for references and generally have fixed voltage potentials during normal operation. Every tiny voltage variation in reference voltages is generally treated as error.

Attached please find a document in the art of reference voltage generator, download from Internet and titled as "Reference Voltage Generator". This document emphasizes that reference voltages are used for comparison with signals and should have fixed voltage potentials. The abstract of *Forbes*, another prior art patent cited by the Examiner, mentions reference voltages several times, each also referring to as a constant voltage according to its corresponding specification. Conclusively, those skilled in the art can not and will not treat voltages for driving data lines as reference voltages.

The Office Action's interpretation of reference voltages is not consistent with the interpretation that those skilled in the art would reach, and, thus, the rejection 35 U.S.C. 102(e) can not be sustained.

Since claim 1, the only independent claim in the present application, is not anticipated by the prior art patents cited by the Examiner, the rejection of lacking novelty for other claims in this application can neither be sustained and should be withdrawn.

Furthermore, the original claim 14 of the application has introduced "a voltage divider to provide the first reference voltage and a third reference voltage." Accordingly to the Office Action, this voltage divider is interpreted as the gate bias control means 52 in Fig. 10 of *Tsuchi*, consisting of constant current 424, NMOS 421, and constant current 423. However, gate bias control means 52 in *Tsuchi* does not divide any voltage, but provides a constant gate-source voltage approaching the vicinity of a threshold-voltage of the NMOS 421 (Ln. 55-58, Cl. 19). Therefore, it divides nothing but results in that the gate voltage of NMOS transistor 422 changes along with the change of Vin. A voltage divider should divide voltage. It is exemplified in Fig. 4 of the present application where serially-connected resisters R_1 and R_2 divide the voltage of V_{cc}, a reference voltage, to generate V_{ref3}, another reference voltage. For at least this additional reason, the rejection of claim 14 should be withdrawn.

In addition, there is no third reference voltage in Fig. 10 of *Tsuchi*. According to the Office Action's interpretation, even if Vin and the voltage at the gate of NMOS 422 are the first and second reference voltages of the present application, the source voltage of NMOS is the same as Vin, the first reference voltage, and can not be interpreted as a third one. Since the limitations of the voltage divider and a third reference are not taught by *Tsuchi*, the 102 rejection of claim 14 should be withdrawn.

Discussion of Rejections Under 35 U.S.C. 103(c)

Similar to *Tsuchi*, the other two prior art patents cited by the Examiner, *Forbes* and *Khalid*, do not disclose the level shifter and the feedback circuit as claimed in claim 1 of the present invention. There is no motivation for the gate voltage of MOS 422 and the voltage of Vin in Fig. 10 of *Tsuchi* to be replaced by two reference voltages with constant voltage potentials. Therefore, neither *Tsuchi*, *Forbes, Khalid*, nor the combination thereof anticipates the claims of the present invention.

For at least the foregoing reasons, Applicant submits that the presently-outstanding rejections to claims 1-14 should be reconsidered and withdrawn.

No fee is believed to be due in connection with this submission. If, however, any fee is deemed to be payable, you are hereby authorized to charge any such fee to deposit account 20-0778.

Respectfully submitted,

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Appendix A

Reference Voltage Generator

A.1 Introduction

In any A/D converters, some reference voltages are generally required to set a reference for the sampled input to be compared to. The accuracy of the reference voltages need to be as linear as the converter itself in most cases. For example, in flash converters, reference voltages are compared with the sampled input signal. Any error present on reference voltages will be added directly to the nonlinearity of the converter. The problem becomes even more severe at high resolution and high speed. In a high speed converter, switching noise on the chip can be coupled onto the reference lines and corrupt the conversion process.

Traditionally, there are two ways to generate reference voltages either by using a resistor string or capacitor array. Each one has its own limitations. It will be shown in Chapter 3 that with some architectural differences, the number of required voltage references has been reduced to two and the tolerance is relaxed with some trimming capacitor.

A.2 Resistor String Voltage Reference Generator

By using multiple passive resistors, one can generate several potential between supply and ground. In the case of a flash converter, the number of reference voltages required is 2^N, where N

is the resolution of the converter. By using 2^N equal value resistors in a string, one can interpolate 2^N different reference potentials between the supply and ground (or full scale input). Two major problems seen at this point are the matching of resistor and high speed operation.

Since the flash converter relies on the absolute value of the reference voltages, mismatch between the resistors during process will cause nonlinearity on the reference voltages. This directly affects the linearity of the output bits. For high resolution, where the LSB size is small, the tolerence on voltage references is even tighter.

For high speed operation, many sampling capacitors might be switched to a reference voltage on the resistor string. This will create a glitch on the refernece, and needs to settle (with the RC time constant) to the required accuracy within the period allowed. The largest RC time constant appears in the center tap of the resistor string, where the equivalent resistor value is $2^{N-1}R \| 2^{N-1}R$ (shown in Figure 1). This transient response causes a signal dependent settling of the DAC and creates harmonic distortion. In order to settle fast enough, small resistor value can be used; however, larger power will be dissipated for the voltage reference generation.

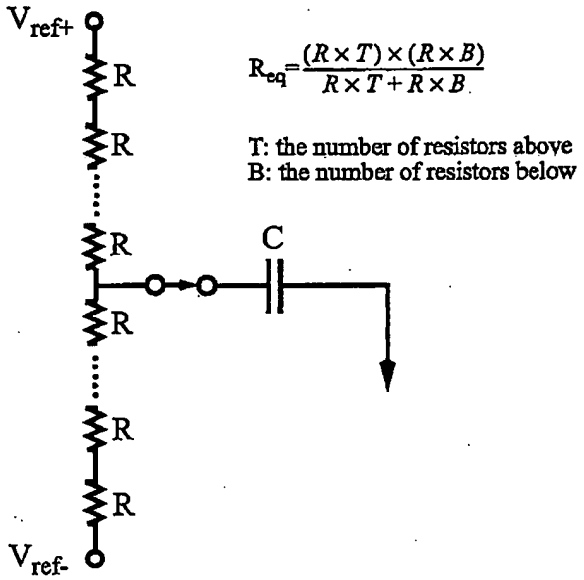

Figure A.1 Time Constant for a tap on the Resistor String

Assuming high power can be tolerated, the mismatch of resistors in the process will still determine the overall linearity of the A/D.

A.3 Capacitor Array Reference Voltage Generator

Another way to generate reference voltages is to use an array of binary weighted capacitors. A family of A/D converters based on this idea is called the successive approximation ADC's. The input is first sampled onto capacitors and then compared with a reference voltage to determine MSB. Then, the quantized MSB is added or subtracted from the input signal to zoom in to next bit resolution.

The typical binary weighted capacitor array is shown in Figure 2. The input is first sampled onto the capacitor array. If $V_{ref} = 0$, the bottom plates of the capacitors are grounded and $-V_{in}$ appears on the top node. However, if one of the capacitor is connected to V_{ref}, the output voltage magnitude will be reduced by the ratio of the specific capacitors to total capacitance times V_{ref} (shown in Figure 2). With this method, V_{ref}'s can be generated equivalently with the capacitor array by connecting various capacitors to the appropriate reference line.

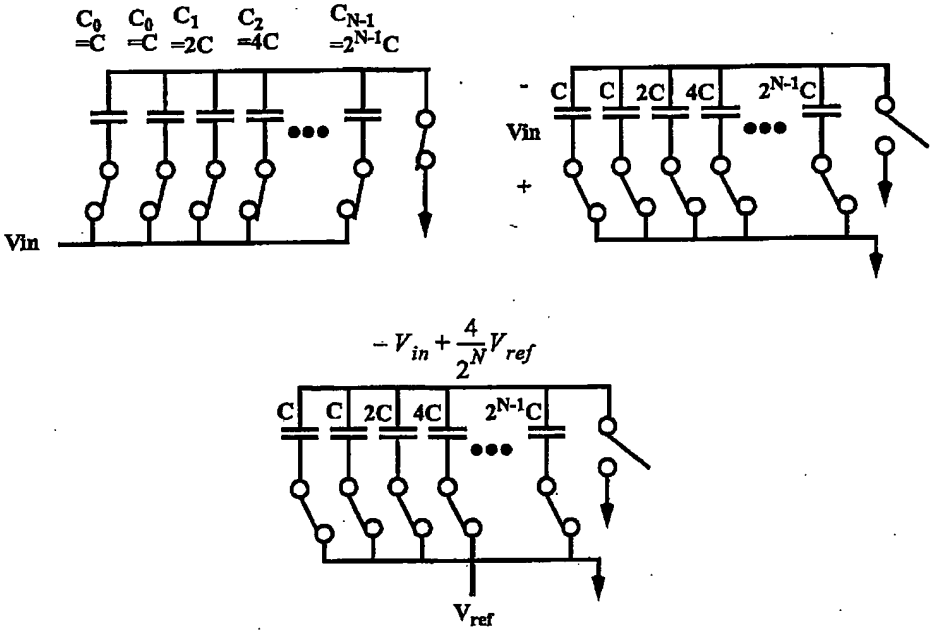

Figure A.2 Capacitor Array Voltage Reference Generator

Although this method does not require static power, the accuracy of the reference generation still relies on the absolute matching of the capacitors. Special techniques have been introduced over the years to improve the matching, however, without special trimming, the achievable resolution is about 8-9 bits.

It will be introduced in later chapters, with some architectural differences, one can eliminate multiple reference voltages and the dependence on the absolute capacitor matching.

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